08:30 Registration	**FPGAworld 2026** Stockholm, September 8th, **AFRY**, Frösundaleden 2A, 169 70 Solna, Sweden		
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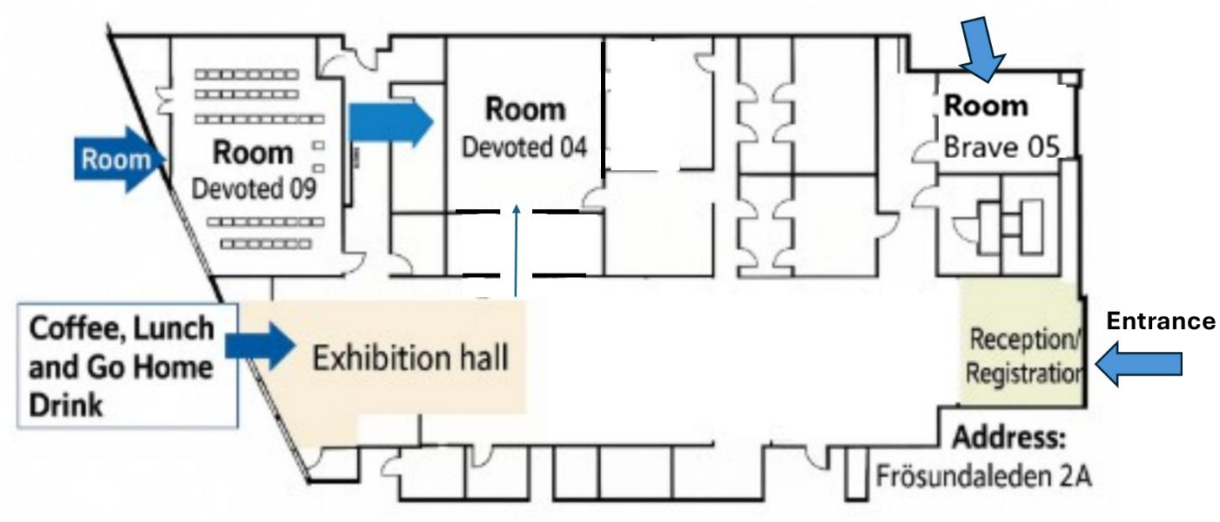
09:00	**Conference Opening** Jihad Daoud, AFRY and Lennart Lindh, FPGAworld/AGSTU **Room:** Devoted 09		
09:15-10:00	**Keynote,** **Title: Su**rvival of the Efficient: Lessons from 40 Years of FPGA Generations and Navigating the Next Decade **Keynote speaker:** Ilya Ganusov is Chief Silicon Architect at Altera, USA **Keynote Chair:** Lennart Lindh, FPGAworld **Room:** Devoted 09 		
10:00-10:25	 **Swedish Fika & Exhibition**		
	Product Track **Session Chair:** **Room:** Devoted 09	**Track:** Altera **Session Organizer and Chair:** Nikolay Rognlien **Room:** Brave 05	**Track** Innofour and Student projects **Session Chair:** Lennart Lindh **Room:** Devoted 04
10:25-11:40 3*25 min	**Title:** Leading Low Power, High Speed Small Form Factor System Devices **Presenter:** Maximilian WernerBooked, Efinix, USA **Title:** From Zero to Secure Edge: Rapid FPGA Development with Pepper Open-Source Development Kit from Pantherun **Presenter:** Michel Pedimina, Pantherun **Title:** GRLIB IP Core library for critical applications **Presenter:** David Esselius, Frontgrade Gaisler, Sweden	**Title:** Agilex™ 5 FPGA with Integrated ARM SoC for Intelligent Edge and Physical AI **Presenter:** Ilya Ganusov **Title:** Inside Agilex™: HyperFlex Core Fabric, Performance, and Power Efficiency **Presenter:** Ilya Ganusov **Title:** End-to-End Robotics with Altera Agilex: Vision, AI, Sensor Fusion, and Control **Presenter:** Angelo Lo Cicero	**Title:** Booked innofour.com **Presenter:** **Junior FPGA Developer, ca 3*16 min** **Title:** NEORV32 – Getting Started with an Open-Source RISC-V Soft-Core on an Altera FPGA **Presenter:** Markus Carlsson, AGSTU Higher Vocational Education, Sweden **Title:** Simulation-First Engineering: Proving a Cycle-Accurate Flash Emulator **Presenter:** Harald Fjellström, AGSTU Higher Vocational Education, Sweden **Title:** SSI Communication in FPGA – Classical and Modified Implementation **Presenter:** Oleksandra Soloviova, AGSTU Higher Vocational Education, Sweden
11:40-12:20	**Lunch Break & Exhibition**		
12:20-13:35 3*25 min	**Track:** VUnit **Session Organizer and Chair:** Lars Asplund **Room:** Devoted 09	**Track:** AMD **Session Organizer and Chair:** Martin Nissmo **Room:** Devoted 04	**Track:** Lattice Semiconductor **Session Organizer and Chair:** Amy Hill **Room:** Brave 05

	Title: Using VUnit to prototype and verify DSP implementations **Presenter:** Ludvig Snihs, Independent, Sweden **Title:** Leveraging LLMs in VHDL verification with Python behavioral models through VUnit **Presenter:** Jonas Julian Jensen, VHDLwhiz **Title:** Beyond VHDL: Bringing the Python Ecosystem into Simulation **Presenter:** Lars Asplund, Synective Labs	**Title:** Highest Security enablement, scaling from AMD FPGAs to Versal SoCs **Presenter:** Neal Frager **Title:** Next Generation SoC Integration with Versal RF **Presenter:** David Taylor **Title:** Automating Vivado with the New AI Extension & Agent Skills **Presenter:** Shuo Hu	**Title:** Solving Your Power Puzzle: Lattice FPGAs' Path to Uncompromised Low Power **Presenter:** Matt Holdsworth **Title:** Role of Low Power FPGAs in physical AI – sensor fusion, compute offloading, and synchronization **Presenter:** Paul Hardy **Title:** **Presenter: Booked** Lattice
13:35-14:00	**Swedish Fika & Exhibition** 		
14:00-15:15 3*25 min 5 min to change room.	**Track:** Open-source tools for FPGA development Session **Session Organizer and Chair:** Oscar Gustafsson **Room:** Devoted 09	**Track:** Microchip **Session Organizer and Chair:** Martin Kellermann and Brian Colgan **Room:** Devoted 04	**Track** **Session Organizer and Chair:** **Room:** Brave 05
	Title: Taping out open-source FPGAs with FABulous and LibreLane **Presenter:** Leo Moser, Universität Heidelberg, Germany **Title:** B-ASIC - a design framework for efficient time-multiplexed implementation of static algorithms **Presenter:** Simon Bjurek, Linköpings universitet **Title:** The open waveform viewer Surfer - now with integrated simulation and collaborative debugging **Presenter:** Oscar Gustafsson, Linköpings universitet	**Title:** FPGA Vision: Bridging and Broadcast **Presenter:** Brian Colgan **Title:** Deterministic Vision and Precision Control Architectures for Humanoid Robot **Presenter:** Brian Colgan **Title:** One Size Does Not Fit All: Power-Efficient Vision AI on FPGAs and Beyond **Presenter:** Martin Kellermann	**Title:** UVVM : The UVM for VHDL – only simpler **Presenter:** Espen Tallaksen, EmLogic, part of TechSeed, Norway **Title:** Distributed processing for accelerated emulation and co-verification of Gemmini NPU **Presenter:** Yehoshua Shoshan, Shevatech AB, Sweden **Title:** From Models to Testbenches: Accelerating FPGA Verification with MATLAB and Simulink **Presenter:** Daniel Aronsson. MathWorks, USA
15:20-16:05	**Keynote,** **Title:** Bitstreams, Backstories & Breakthroughs: A Security Journey in FPGAs **Keynote speaker:** Martin Kellermann, Microchip Technology GmbH, Munich, Germany **Keynote Chair:** Lennart Lindh, FPGAworld/AGSTU **Room:** Devoted 09 		
16:05 -	**Go Home Drink in the Exhibition Hall and Welcome to FPGAworld next year!** FPGA™ world		

More information



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Keynotes FPGAworld Stockholm

Title: Survival of the Efficient: Lessons from 40 Years of FPGA Generations and Navigating the Next Decade
Keynote speaker: Ilya Ganusov is Chief Silicon Architect at Altera

Abstract: FPGA architectures have undergone repeated redesign cycles, shaped by the relentless pressure of semiconductor limits, shifting market demands, and the practicalities of deployment. While certain architectural concepts have successfully scaled across generations, others have faltered despite some initial promise.
In this keynote, we will examine the historical trajectory of FPGA performance and power metrics, but we will ultimately argue that cost in its many dimensions is the ultimate architect. We will explore how the “invisible hand” of cost has quietly dictated the evolution of logic fabrics, routing complexity, and the strategic integration of hardened IPs. From silicon floorplans to the inherent complexities of software toolchains, successful innovation has consistently hinged on finding the optimal economic and technical trade-offs.
By extracting these durable lessons, we can better navigate the next decade of reconfigurable computing. We will examine how a cost-centric mindset – one that balances area, power, development time, and software friction – remains our most powerful tool for uncovering new opportunities for FPGAs in an increasingly complex semiconductor landscape.

CV: Ilya Ganusov is Chief Silicon Architect at Altera, leading FPGA architecture definition and long term architectural research across core fabrics, memory and interconnect architectures, and architectural methodologies under real world power and performance constraints. He joined Intel's FPGA organization in 2018, where he led the Agilex™ FPGA core architecture and application driven optimizations for AI, high performance computing, wireless communications, and real time systems. Prior to Intel and Altera, he held senior architecture roles at Xilinx, contributing to multiple FPGA generations, and at Achronix, working on asynchronous FPGA architectures. Ilya has co authored more than 40 granted patents and numerous publications on FPGA architectures, CAD algorithms, memory systems, and circuit design. He holds a Ph.D. in Electrical and Computer Engineering from Cornell University.

Title: Bitstreams, Backstories & Breakthroughs: A Security Journey in FPGAs
Keynote speaker: Martin Kellermann, Microchip Technology GmbH, Munich, Germany

Abstract: Security in FPGAs didn't arrive as a monolith. It evolved across generations as we learned what attackers cared about and what users needed. This talk traces that evolution from our antifuse roots, through authenticated configuration and side channel resistant provisioning, to today's layered, defense grade feature sets that make security a built in property rather than an add on.
Along the way we'll share compact, technical stories that changed our trajectory, like the polite note from an independent lab demonstrating device key extraction via differential power analysis. That single data point galvanized a shift to DPA resistant cryptography and third party evaluation, and it shaped how we think about key storage, tamper response and zeroization.
Attendees will leave with a practical timeline of "what, why, and how" of authenticated bitstreams, DPA hardened flows, PUF anchored key custody, tamper sensors with deterministic zeroize and secure provisioning chains and guidance on when each control matters. It's a candid, engineering level look at how trustworthy FPGAs are built and how those lessons transfer to your next design.

CV: Martin Kellermann is a Marketing Manager at Microchip Technology GmbH, Munich. In this role he works with the European Sales and Field Application team to position the strengths of Microchip FPGAs and SoCs to clients.
He is a seasoned FPGA and SoC professional with a track record of successful customer and project engagements in the industrial, automotive, and data-center domains. Martin possesses a strong background in high-speed serial data transmission, signal integrity and hardware debugging which helped numerous customers finish their designs successfully. He has also taught courses covering industrial applications and hardware concepts. Martin holds a diploma on Electrical Engineering from the Landshut University of Applied Sciences.

Other presentations

Title: UVVM : The UVM for VHDL – only simpler
Presenter: Espen Tallaksen, EmLogic, part of TechSeed, Norway
Abstract:
UVVM is currently being used by 27% of all FPGA designers and 25% of all ASIC designers worldwide - and increasing. This is due to the improvement in UVVM yields in both FPGA quality and development time. This open-source Library and Methodology have the most extensive VHDL verification support available and lets you verify complex DUTs in a very efficient manner, providing overview, readability, modularity, reusability, and debuggability similar to UVM, but far simpler to use.
UVVM has been significantly updated through several ESA (European Space Agency) UVVM extension projects over the last few years, and we are currently working on even more new features - in tight cooperation with ESA.
UVVM provides a testbench kick start with open source BFMs and verification components for UART, SPI, AXI, AXI-lite, APB, AXI stream, Avalon MM + Stream, I2c, GPIO, SBI, GMII, RGMII, Ethernet, Wishbone, Clock generator, and Error injector.
You also have all the other functionality you need for your testbench, like Requirements Tracking, Enhanced Randomisation, Functional Coverage, Scoreboards, Error Injection, etc.
And if you have a simple DUT, then you just use the basic parts of UVVM.
This presentation will give you a brief introduction to UVVM - but also show the most important features and explain how they will help you make a better testbench and develop this much faster.

Title: GRLIB IP Core library for critical applications
Presenters: David Esselius, Frontgrade Gaisler, Sweden
Abstract:
This presentation highlights Gaisler's transformative solutions for FPGA applications: the GRLIB IP Library and the NOEL RISC-V processor line. The GRLIB IP Library offers a modular suite of IP cores optimized for easy integration, while NOEL-V provides a fault-tolerant RISC-V processor tailored for critical applications. Building on this, NOEL3 introduces advanced features for real-time processing. Together, these products empower engineers to quickly develop reliable, high-performance systems.

Title: Using VUnit to prototype and verify DSP implementations
Presenter: Ludvig Snihs, Sweden
Abstract:
Prototyping and verification of digital signal processing (DSP) algorithms can be carried out efficiently in Python prior to hardware implementation. The availability of structured debugging, numerical analysis, and visualization facilitates early-stage validation and identification of functional discrepancies. A Python-based reference model can subsequently be used during FPGA verification to support consistency between algorithmic intent and hardware realization.
This presentation outlines a workflow based on VUnit, where Python models are integrated into the verification process. Pre-configurations enable execution of the reference model, while post-checks are used to identify deviations from expected behavior. The approach also allows extraction of quantitative data, such as signal traces and performance-related metrics, for further analysis.
A set of DSP implementations is presented, following a progression from theoretical formulation to Python modeling and FPGA implementation. The examples include:

- Polyphase filters
- Finite impulse response (FIR) filters with variable cutoff frequency
- Halfband filters
- Cascaded integrator-comb (CIC) filters
- CORDIC-based computational structures
- Fast Fourier Transform (FFT)

The methodology is illustrated through a complete FPGA-based system, implemented on Zybo Z7-10, demonstrating how the approach can be applied to a coherent DSP application.

Title: The open waveform viewer Surfer - now with integrated simulation and collaborative debugging **Presenter:** Oscar Gustafsson, Linköpings universitet
Abstract:

Surfer is an open-source waveform viewer that runs on all common platforms that is built to be flexible and extendable. Recently, there has been support added for integrating with simulators. Currently, the open-source simulator NVC is supported, which is a VHDL simulator that also has some basic Verilog support, although support for other simulators are planned. Annotations is another feature recently added, where multiple users can connect to the same waveform database and share annotations in real-time, avoiding screen sharing and/or sending screen shots. These and other features of Surfer will be presented.

Title: Highest Security enablement, scaling from AMD FPGAs to Versal SoCs
Presenter: Neal Frager
Abstract:
This session introduces the security capabilities of AMD FPGAs & adaptive SoCs. From the moment power is applied through the release of critical design information and runtime applications, AMD FPGA/SoCs have the capability to provide authenticity, confidentiality, and integrity of our customers' IP and data.

Title: Next Generation SoC Integration with Versal RF
Presenter: David Taylor
Abstract:
This presentation provides an overview of the AMD Versal™ RF Series, showcasing its next-generation high-performance data converters that deliver unprecedented sampling rates, wider RF bandwidth, and advanced on-chip signal-processing capabilities. Gain a clear understanding of the architecture, features, and advantages of the integrated RF-ADC, RF-DAC, and DSP hard IP, which will enable industry-leading compute efficiency.

Title: Automating Vivado with the New AI Extension & Agent Skills
Presenter: Shuo Hu
Abstract:
Agentic AI is revolutionizing FPGA development by addressing critical challenges in the design cycle. Using a natural-language-driven workflow, Agentic AI facilitates multiple stages of FPGA development, from interpreting design intent to generating hardware and software artifacts. This session outlines how Agentic AI streamlines design analysis and closure, ensuring timing accuracy and thereby reducing complexity and time. By advocating for a modern, software-centric approach, we illustrate how Agentic AI enhances the accessibility and efficiency of FPGA development for engineers across the board.

Title: Leading Low Power, High Speed Small Form Factor System Devices
Presenter: Maximilian Werner
Abstract:
Efinix offers FPGAs in a small form factor that can serve as system controllers, ideally suited for demanding edge applications. The new System in Package (SiP) devices further simplify integration by combining multiple advantages such as lower power consumption, a smaller footprint, and easier PCB integration. Examples include the Ti125 SIP with integrated HyperRAM and the Ti135 SIP with integrated LPDDR4. These devices deliver unprecedented performance in terms of speed and power efficiency. This presentation provides a detailed overview of the new devices and their features, along with exemplary applications

Title: FPGA Vision: Bridging and Broadcast
Presenter: Brian Colgan
Abstract:
Modern embedded vision systems demand high-bandwidth sensor and video interfaces with deterministic, low-latency processing at the edge.
This presentation explores FPGA-based vision architectures supporting HDMI, SDI, SLVS-EC, and CoaXPress, including HDMI-to-SDI conversion and quad CoaXPress capture. We examine how FPGAs enable flexible interface bridging, real-time image processing, and scalable high-resolution pipelines while meeting strict power, reliability, and timing requirements.

Title: Deterministic Vision and Precision Control Architectures for Humanoid Robot
Presenter: Brian Colgan

Abstract:
Humanoid robots are moving toward scalable, Ethernet-based architectures that support stereo depth perception, distributed cameras, and real-time intelligence. Microchip PolarFire® FPGAs, integrated with NVIDIA Holoscan, provide a complete solution for vision and precision motor control in next-generation humanoid systems.
We will show how to implement a power-efficient, deterministic pipeline for synchronized stereo and multi-camera vision, leveraging high-bandwidth SerDes and flexible protocol support to transport time-aligned image data over Ethernet into NVIDIA Holoscan for AI-driven perception and sensor fusion. In parallel the highly dexterous manipulators require deterministic low-latency motor control which can only be achieved using FPGAs. Talking of controlling hands, 20+ degrees of freedom may be required to deliver the precision and accuracy needed for human-like motion.
Together, the combination of FPGA and GPU offer a scalable, standards-based architecture that unifies depth perception, distributed vision, and ultra-low-latency control in power-constrained humanoid platforms.

Title: One Size Does Not Fit All: Power-Efficient Vision AI on FPGAs and Beyond
Presenter: Martin Kellermann
Abstract:
Embedded AI deployments span a wide range of performance, power, and integration constraints, yet they are often approached with a “one-size-fits-all” mindset. This talk argues that such an approach is as inefficient as using a 40-ton truck for weekly grocery shopping. Instead, we explore how tailoring AI architectures to the actual workload can unlock significant gains in efficiency and throughput. We focus on power-efficient AI processing for vision data on FPGAs and FPGA-SoCs highlighting architectural trade-offs and design considerations. A key enabler is unstructured sparsity: using tools from Neuronix, who were acquired by Microchip, pruning is performed during training to produce a sparse neural network that is then processed by Neuronix tools for sparsity removal. This transforms it into a hardware-efficient implementation without sacrificing accuracy. Additionally, we position FPGA-based embedded AI within a broader heterogeneous compute landscape, showing how workloads can scale toward higher-end solutions using NVIDIA Holoscan IP when application complexity or data rates exceed embedded constraints. The result is a pragmatic, scalable view of AI acceleration, from an efficient edge inference to high-performance systems, where the right tool is used for the right job.

Title: From Zero to Secure Edge: Rapid FPGA Development with Pepper Open-Source Development Kit from Pantherun
Presenter: Michel Pedimina, Pantherun
Michel Pedimina brings over 25 years of expertise in secure telecommunications and mission-critical systems to his role as Principal Engineer at Pantherun. With a distinguished background leading largescale integrations for rail and telecom giants like SBB, Deutsche Bahn, and Swisscom, Michel possesses the precise operational insight required to deploy Pantherun’s Edge AI and security solutions into critical infrastructure environments. He combines deep technical mastery of cybersecurity and industrial IoT with hands-on architectural leadership, positioning him to drive the technical vision of the Pepper platform and bridge the gap between high-performance FPGA hardware and the rigorous demands of secure, zero-trust edge applications.

Abstract:
FPGAs have traditionally been the domain of specialized hardware engineers. Pantherun has changed the game. This 30 minute workshop will demonstrate the ease-of-use and power of the Pepper open-source FPGA platform. By the end of the session, attendees will learn the basics on how to deploy hardware-accelerated applications using software tools with the guidance and training of Pantherun experts. In addition, attendees will have a Pepper board presented to them that’s theirs to keep.
Attendees will get hands-on experience and tech support with:

- **Board Bring-up:** How to boot and configure the Pepper platform from scratch.
- **FPGA-as-a-Service:** Understanding how to load FPGA bitstreams dynamically from Linux.

After the session, attendees will also be provided with a guide where they will be able to build a "Smart Secure Gateway" application that takes data, encrypts it in real-time, and transmits it over Ethernet/Wi-Fi.

Title: Distributed processing for accelerated emulation and co-verification of Gemmini NPU
Presenter: Yehoshua Shoshan, Shevatech AB, Sweden
Abstract:
Using a distproc an IPC based platform for distributed processing one can connect and synchronize processes of different

kind. In this presentation I will show how connecting a python orchestrator to a swarm of Gemmini NPUs enable hardware/firmware co verification.

Title: Taping out open-source FPGAs with FABulous and LibreLane
Presenter: Leo Moser, Universität Heidelberg, Germany
Abstract:
FABulous is an easy-to-use, silicon-proven, open-source (e)FPGA generator. Together with LibreLane, a powerful and versatile ASIC infrastructure library for open-source and commercial EDA tools, it is possible to design a fully open-source FPGA implementation down to the silicon level.
In this talk, I will provide an overview of the chips that I taped out using FABulous and LibreLane on various processes, such as SKY130A, GF180MCU and IHP-SG13. I will discuss the challenges I encountered and showcase a silicon demonstration

Title: Beyond VHDL: Bringing the Python Ecosystem into Simulation.
Presenter: Lars Asplund, Synective Labs
Abstract: VHDL simulations have traditionally been isolated worlds, largely disconnected from the vast software ecosystems available today. What happens when a simulation can directly access Python and everything that comes with it?
This presentation introduces our work with a new VUnit package that enables straightforward and seamless interaction between VHDL and Python during simulation. By opening a bridge between the two languages, verification environments can leverage capabilities that would otherwise be difficult or impractical to implement in VHDL alone. We will demonstrate examples from advanced visualization, data analysis, hardware in the loop simulations, interactive user interfaces, and more.

Title: Leveraging LLMs in VHDL verification with Python behavioral models through VUnit
Presenter: Jonas Julian Jensen, VHDLwhiz
Abstract: Large language models (LLMs) are getting better at VHDL, but there's still a long way to go before we can ask chatbots to auto-generate full FPGA systems. A lot of that comes down to HDLs being far less common than programming languages on the internet, and thereby underrepresented in their training data.
Python code is far more prevalent, and as a consequence, generative AI is very good at coding it. One way to make use of that in VHDL design is to offload verification work to Python, as VUnit already allows. This presentation takes it further by showing how to use AI-generated Python behavioral models for verifying VHDL RTL modules.
This speeds up development, and a behavioral model written by a different author (the LLM) in a different language may reveal bugs that a single-author VHDL testbench could repeat.

Title: Solving Your Power Puzzle: Lattice FPGAs' Path to Uncompromised Low Power
Presenter: Matt Holdsworth
Abstract: Tired of compromising performance for power efficiency? This session reveals the engineering breakthroughs behind Lattice FPGAs' industry-leading low power consumption. We'll explore our unique approach, showcasing how innovations across silicon process, architecture, and design methodologies culminate in FPGAs that significantly reduce system power. Understand the technical advantages that empower you to design smaller, cooler, and more energy-efficient solutions, all while maintaining the high performance your applications demand.

Title: Role of Low Power FPGAs in physical AI – sensor fusion, compute offloading, and synchronization
Presenter: Paul Hardy
Abstract: The physical AI grows fast with more intelligence in the form of robot that is composed of sensors, computing engine (CPU/GPU), and actuators. CPU/GPU gets raw data from sensors over high-speed network, processes, and makes high-level decisions. But, as the number of sensors increases, the low-level processing of raw data becomes a larger task that burns sizable computing resources, and the network also becomes crowded with more raw data. This becomes a limiting factor for the use of more sensors. The synchronization of actuators becomes an issue too as the number of actuators grows, while low & deterministic synchronization is needed in modern robots. Lastly, chips need to work in a tighter and enclosed area with not much air flow in robots, and it makes the heat dissipation much harder.
To tackle these issues, we are using low power FPGA. It is located near to sensors to sync, fuse, and process the data before sending over network. It reduces the computing burden of CPU/GPU so that it can do intelligent task instead of low-level computing and the network bandwidth since it sends digested data. FPGA is used for the communication for

sync of actuators, and it gives deterministic & low latency compared to the MCU based solutions. Lastly, the less heat from the low power FPGA removes the need for any fan or heat sink, which is essential for a tight closed environment. These benefits of FPGAs make robots more intelligent and work long without extra cost on CPU/GPU and battery.

Title: From Models to Testbenches: Accelerating FPGA Verification with MATLAB and Simulink
Presenter: Daniel Aronsson is a principal application engineer at MathWorks with specialization in signal processing and communications system design. He has 20 years of experience in these fields, and he also works regularly with Neural Nets and FPGA/ASIC design and verification. Daniel holds a Ph.D. in wireless communications from Uppsala University, on the topic of MIMO channel prediction.
Abstract: As the complexity of modern FPGA designs escalates, traditional HDL verification increasingly becomes a development bottleneck. This presentation demonstrates how to bridge the gap between high-level algorithmic design and hardware implementation by leveraging MATLAB and Simulink for automated verification.
We will explore methodologies to accelerate the verification pipeline, including generating reusable HDL testbenches directly from golden reference models, utilizing HDL Cosimulation (with ModelSim/Questa) to catch bugs early, and implementing FPGA-in-the-Loop (FIL) testing to validate algorithms on physical hardware at speed. Attendees will learn how to transition seamlessly from mathematical modeling to robust hardware verification, significantly reducing time-to-market and eliminating manual testbench errors.

Title: B-ASIC - a design framework for efficient time-multiplexed implementation of static algorithms
Presenter: Simon Bjurek, Linköpings universitet
Abstract: B-ASIC is a Python framework providing a design path for the case where you have a static algorithm and a given sample rate that is a integer or rational multiple of the system clock. The framework will help you in simulating the algorithm and assist in deriving an efficient time-multiplexed architecture, for which code and test benches can be generated. A bit like HLS, but with complete control of every design step.

Title: NEORV32 – Getting Started with an Open-Source RISC-V Soft-Core on an FPGA
Presenter: Markus Carlsson, AGSTU Higher Vocational Education, Sweden
Abstract: The NEORV32 Processor is an open-source RISC-V soft-core which comes as a complete and customizable system on chip (SoC) solution. The open-source project is designed in VHDL and is intended to work out of the box on any FPGA platform. This talk provides a practical introduction to NEORV32, covering the RISC-V GCC toolchain, some of NEORV32 basic components and its bootloader. It will be implemented on a DE10-Lite board with a MAX 10 FPGA and synthesized in Quartus Prime. The talk will end with a live demo running on hardware with demo code provided by the NEORV32 project. Attendees will leave this talk with a starting point to explore RISC-V soft-cores on their own and begin their own FPGA projects.

Title: Simulation-First Engineering: Proving a Cycle-Accurate Flash Emulator
Presenter: Harald Fjellström, AGSTU Higher Vocational Education, Sweden
Abstract: While standard FPGA curricula heavily rely on vendor-specific EDA suites, specialized engineering tasks often require looking beyond traditional tooling. This presentation shares an early proof-of-concept developed during a thesis project at Ericsson, focusing on an FPGA-based drop-in emulator for NOR flash memory to safeguard sensitive boot images in volatile RAM.
The session outlines the hardware constraints that guided device selection, prioritizing a solution that avoided adding hardware complexity to the existing platform. To ensure exact cycle accuracy before physical hardware was available, a software-inspired, multi-language simulation framework was implemented. This architecture allowed a single, shared test environment to simultaneously validate the VHDL design against a vendor-provided SystemVerilog reference model. Finally, the talk demonstrates how a flexible, Makefile-driven build system allows the framework to easily adapt to different host microcontrollers and alternative flash boot sequences.

Title: SSI Communication in FPGA – Classical and Modified Implementation
Presenter: Oleksandra Soloviova, AGSTU Higher Vocational Education, Sweden
Abstract: This presentation describes the implementation and verification of two FPGA-based SSI communication solutions: a classical SSI protocol implementation and a modified SSI variant developed as part of an internship project. It provides a brief introduction to the SSI protocol and its industrial applications, followed by an overview of the FPGA design process. The main focus is on the architectural and functional differences between the classical and modified SSI implementations, as well as the challenges encountered during design, simulation, verification, and hardware testing.